Hardware Implementation Example
Anybus CompactCom M40 16 bit mode
Atmel ARM ATSAM3U1EA

History

Revision	Date	Description	Responsible
0.99	2014-10-20	First draft	joka
1.00	2015-06-08	First official version	joka, kel

Contents

1 Requirements

Hardware
Anybus CompactCom M40
AT91SAM ARM-based Flash MCU

Documentation	Document number	Version
Anybus CompactCom M40 Hardware Design Guide	HMSI-216-126	1.31
AT91SAM ARM-based Flash MCU, SAM3U Series. Datasheet	6430F-ATARM	21-Feb-12

2 Solution Overview

This is a description of how to create a design for Anybus CompactCom M40 using 16-bit parallel mode with the Atmel ARM MCU ATSAM3U1EA. This CPU has a Static Memory Controller that does not use bit A0 for 16-bit data bus. When the Anybus CompactCom is configured for 16 bit mode input A0 of the Anybus CompactCom is not used as address input but as /WE input for the high byte. The lowest address input for addressing a 16 bit value is A1. How the hardware signals shall be connected can be seen in Figure 1.

This document is a complement to the Anybus CompactCom M40 Hardware Design Guide.

2.1 Reference information from Atmel Datasheet

The Atmel controller supports two different access modes: byte write access and byte select access.

In this application note the byte write access is illustrated.

Extract of the Atmel Datasheet:

25.9.1 Data Bus Width

A data bus width of 8 or 16 bits can be selected for each chip select. This option is controlled by the field DBW in SMC_MODE (Mode Register) for the corresponding chip select.

25.9.2 Byte Write or Byte Select Access

Each chip select with a 16-bit data bus can operate with one of two different types of write access: byte write or byte select access. This is controlled by the BAT field of the SMC_MODE register for the corresponding chip select.

25.9.2.1 Byte Write Access

Byte write access supports one byte write signal per byte of the data bus and a single read signal.

Note that the SMC does not allow boot in Byte Write Access mode.

- For 16-bit devices: the SMC provides NWR0 and NWR1 write signals for respectively, byte0 (lower byte) and byte1 (upper byte) of a 16-bit bus. One single read signal (NRD) is provided.

Table 25-1. I/O Line Description

Name	Description	Type	Active Level
NCS[3:0]	Static Memory Controller Chip Select Lines	Output	Low
NRD	Read Signal	Output	Low
NWR0/NWE	Write 0/Write Enable Signal	Output	Low
A0/NBS0	Address Bit 0/Byte 0 Select Signal	Output	Low
NWR1/NBS1	Write 1/Byte 1 Select Signal	Output	Low
A1	Address Bit 1	Output	Low
A[23:2]	Address Bus	Output	
D[15:0]	Data Bus	I/O	
NWAIT	External Wait Signal	Input	Low
NANDRDY	NAND Flash Ready/Busy	Input	
NANDWE	NAND Flash Write Enable	Output	Low
NANDOE	NAND Flash Output Enable	Output	Low
NANDALE	NAND Flash Address Latch Enable	Output	
NANDCLE	NAND Flash Command Latch Enable	Output	

3 Application Note

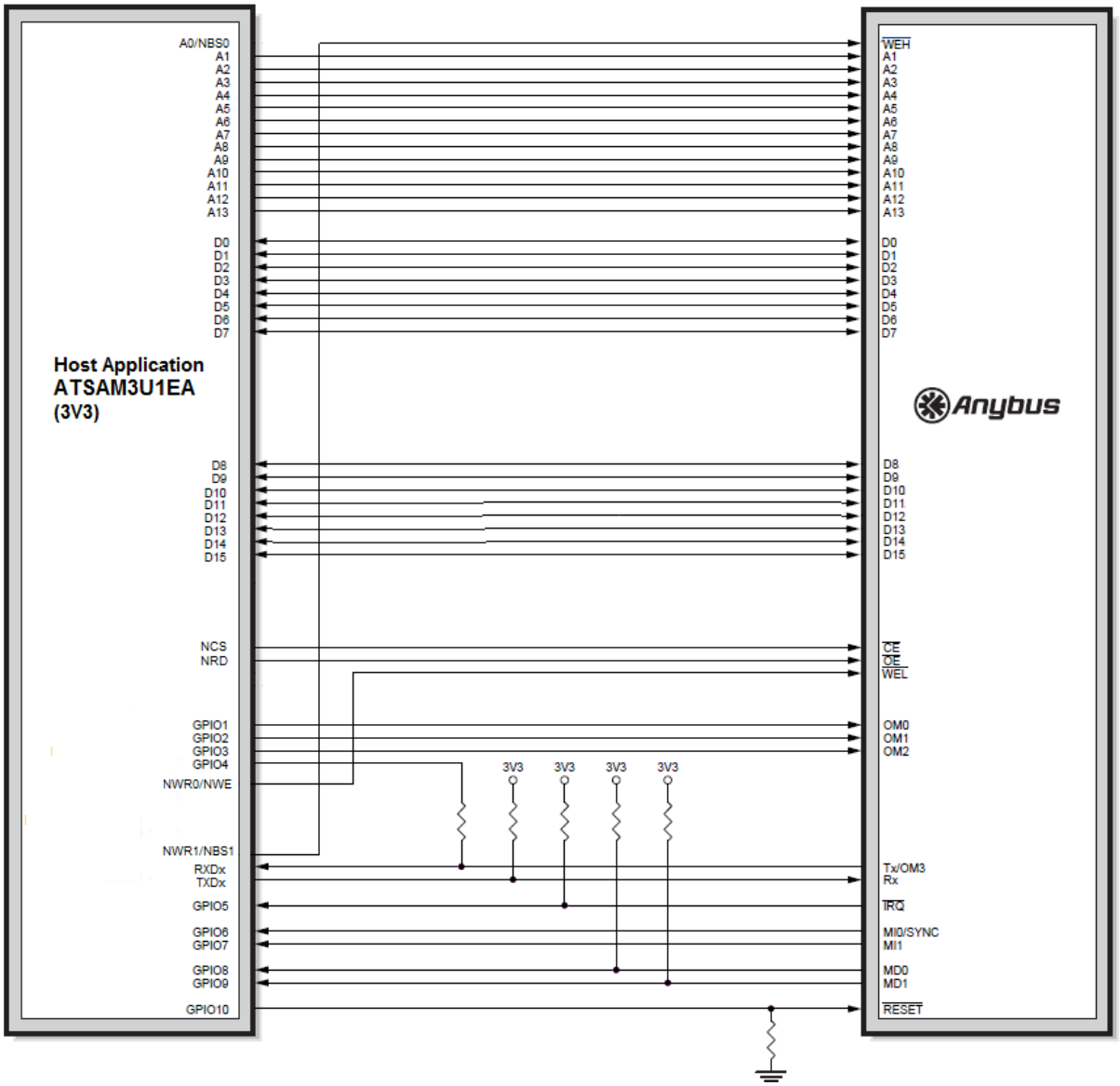

Figure 1 Hardware implementation example of using the Anybus CompactCom in 16 bit mode connected to an Atmel ARM CPU, ATSAM3U1EA

4 More Information about the Network and Products

The latest manuals, can be found on HMS homepage, www.anybus.com.